

FIG.1A

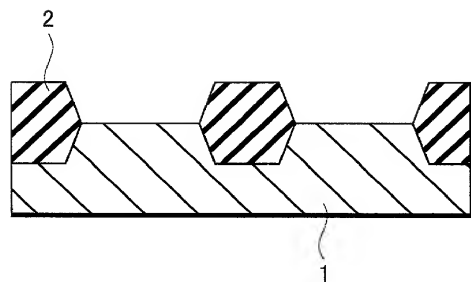


FIG.1B

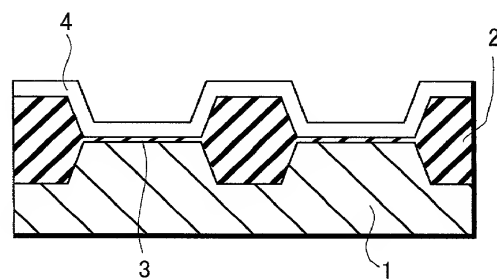


FIG.1C

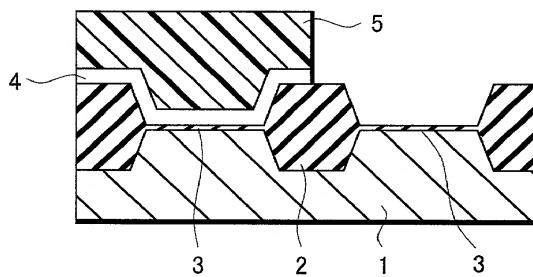


FIG.2A

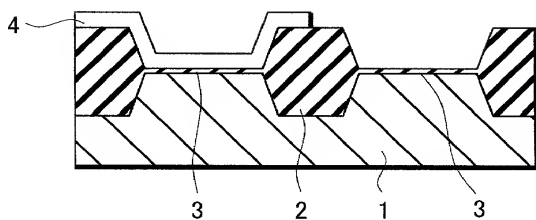


FIG.2B

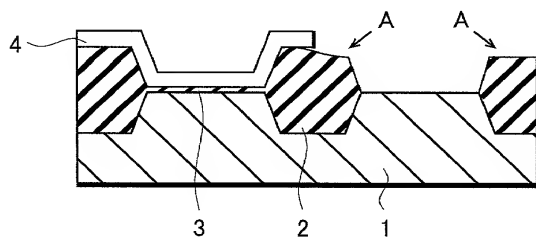


FIG.2C

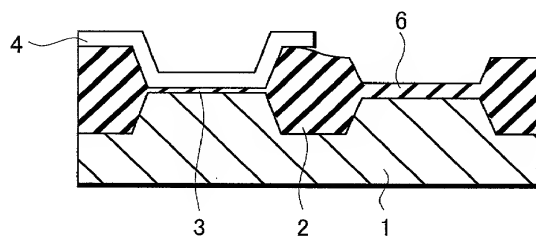


FIG.3A

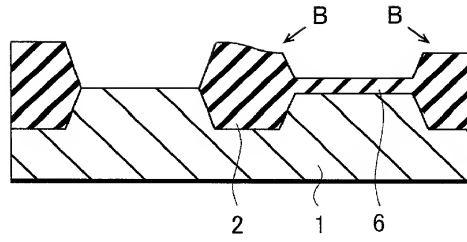


FIG.3B

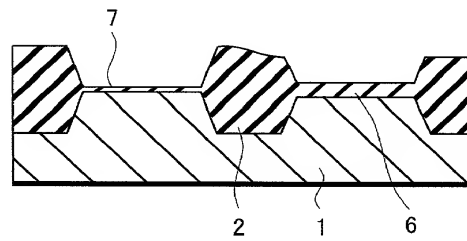


FIG.3C

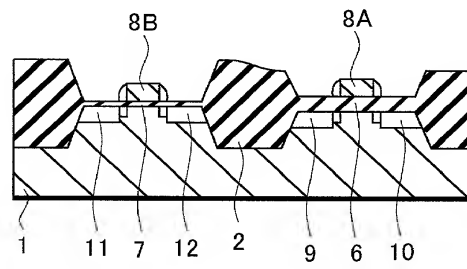


FIG. 4A

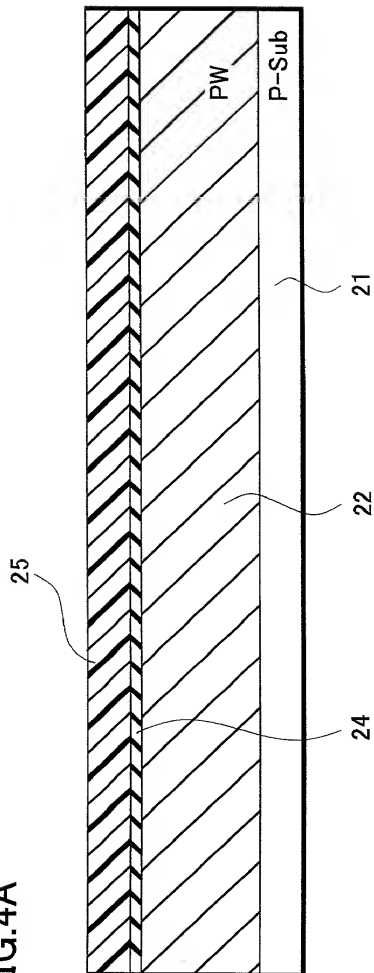


FIG. 4B

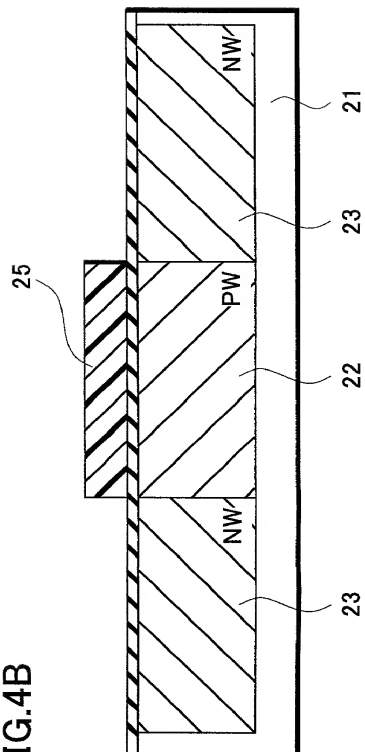


FIG. 5A

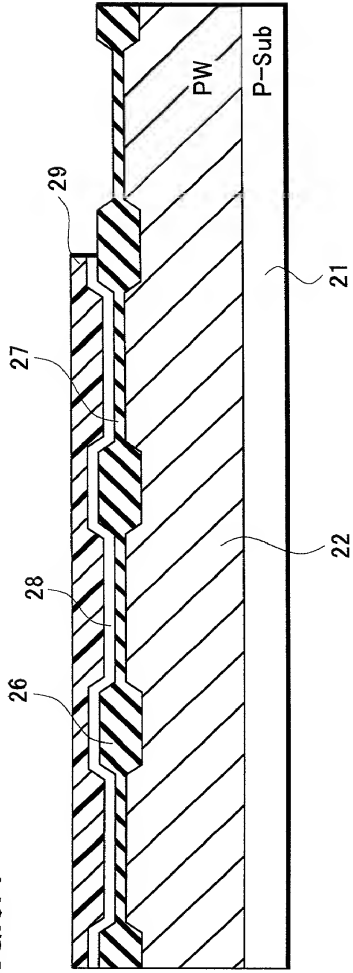


FIG. 5B

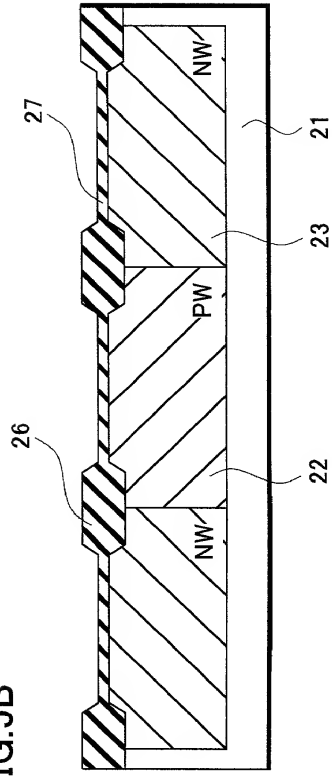


FIG. 6A

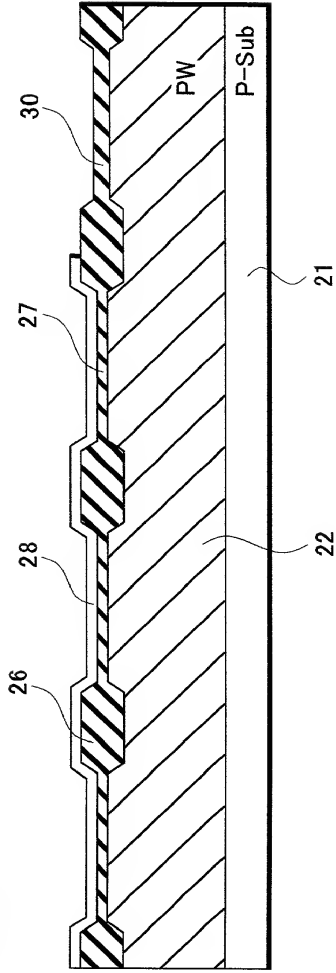


FIG. 6B

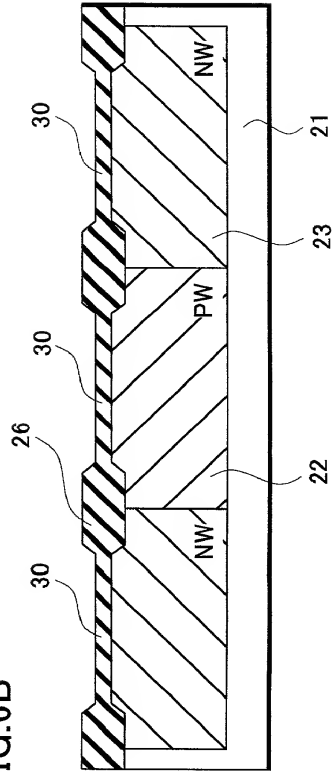


FIG.7A

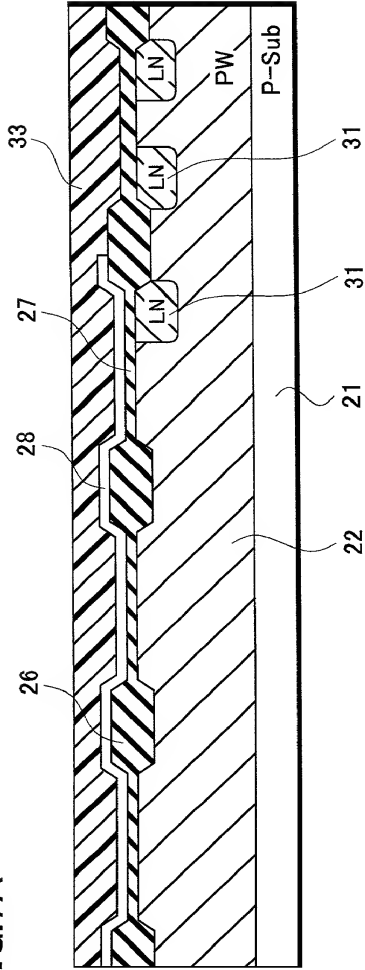


FIG.7B

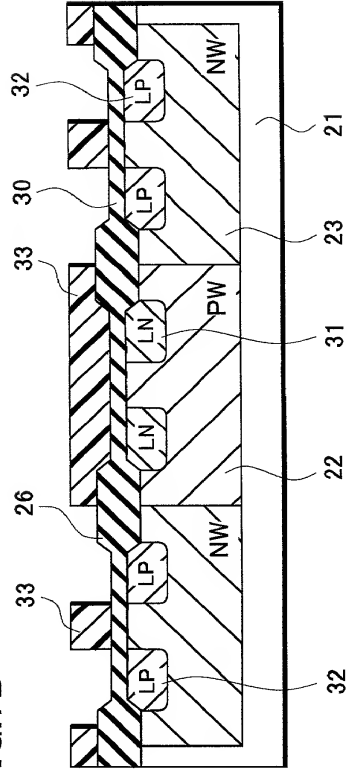


FIG. 8A

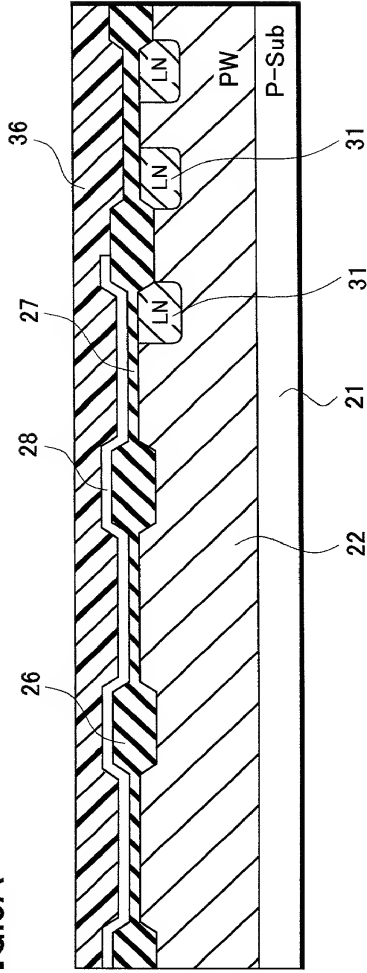


FIG. 8B

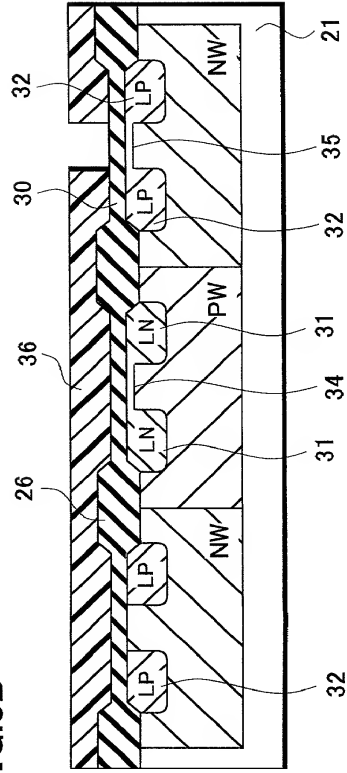




FIG.9A

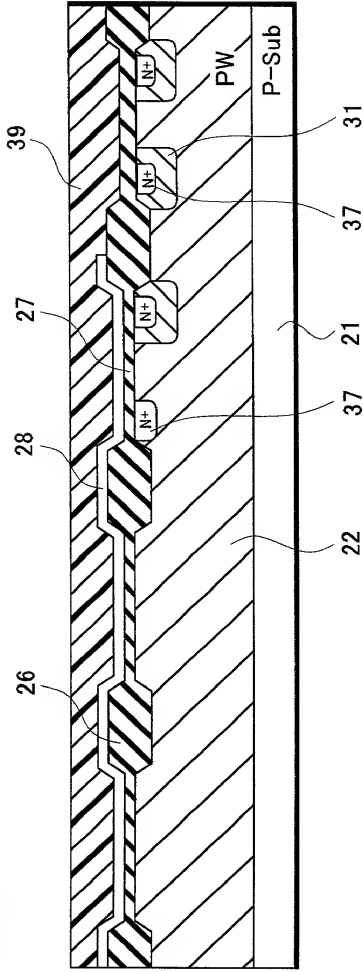


FIG.9B

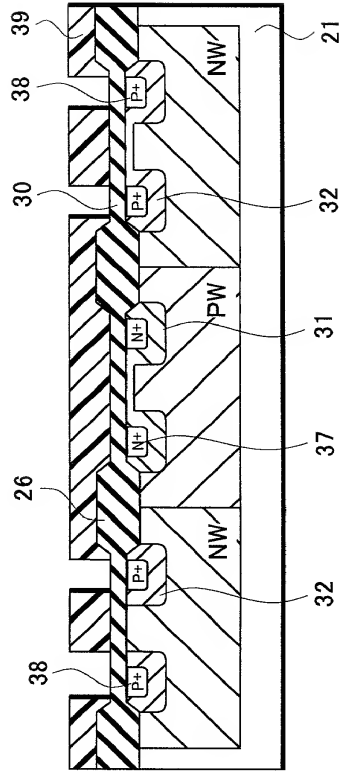


FIG.10A

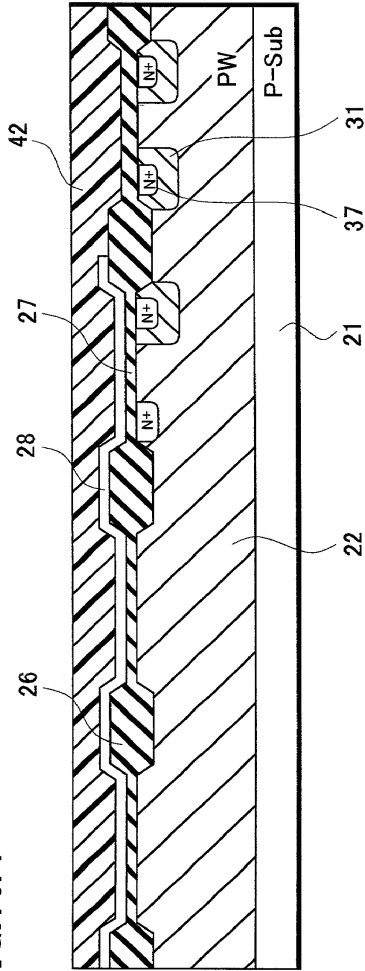
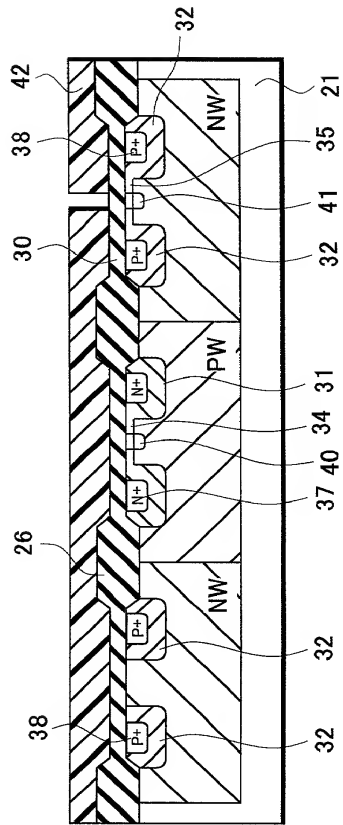


FIG.10B



This cross-sectional view illustrates a semiconductor device structure. A P-Substrate (31) is shown at the bottom, containing a P-type well (PW) and several N+ regions (30, 37). The device is built upon a series of alternating layers (26, 27) and a top layer (31). The layers are labeled with reference numerals 26, 27, 30, 31, 37, and PW.

[illegible]

FIG. 12A

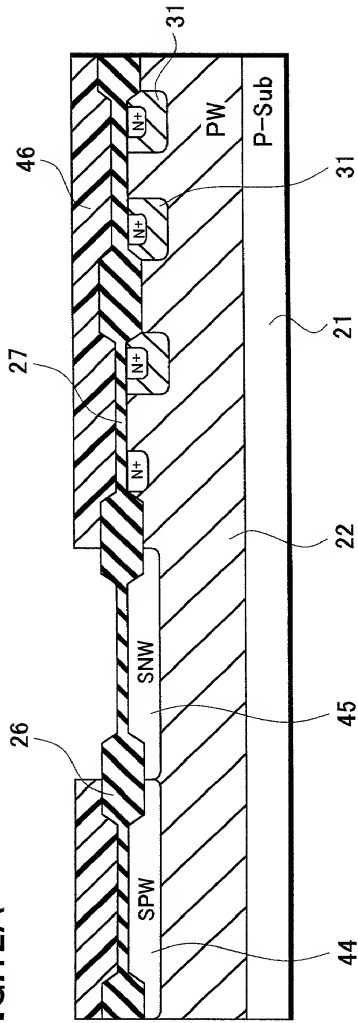


FIG. 12B

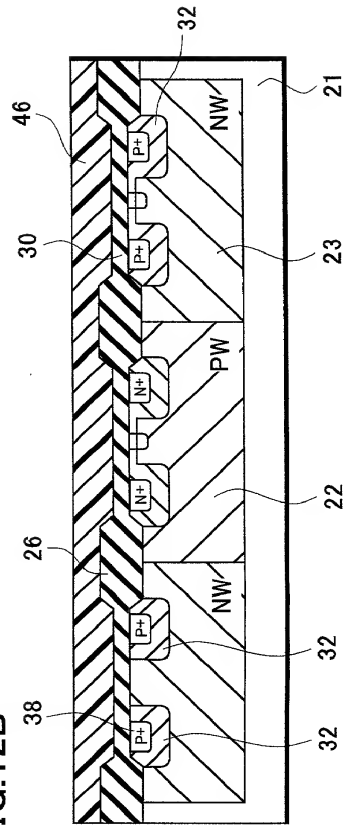


FIG. 13A

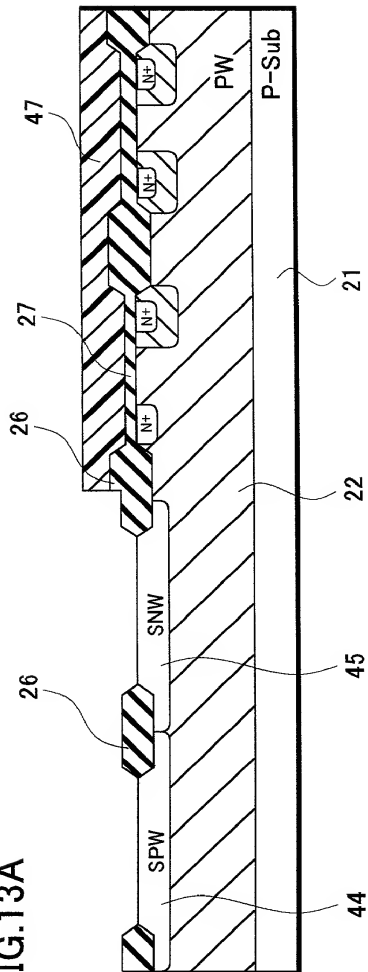


FIG. 13B

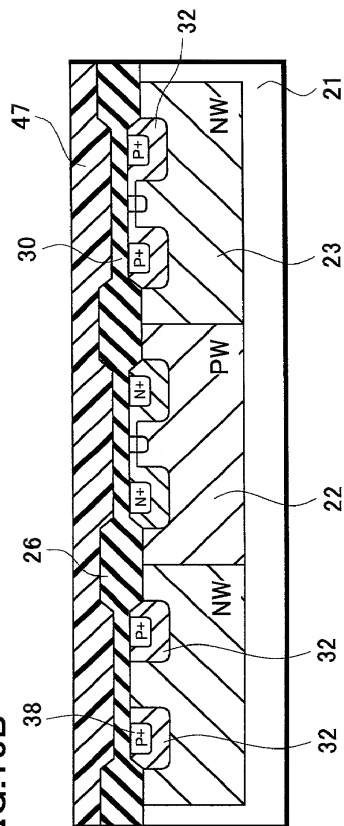


FIG. 14A

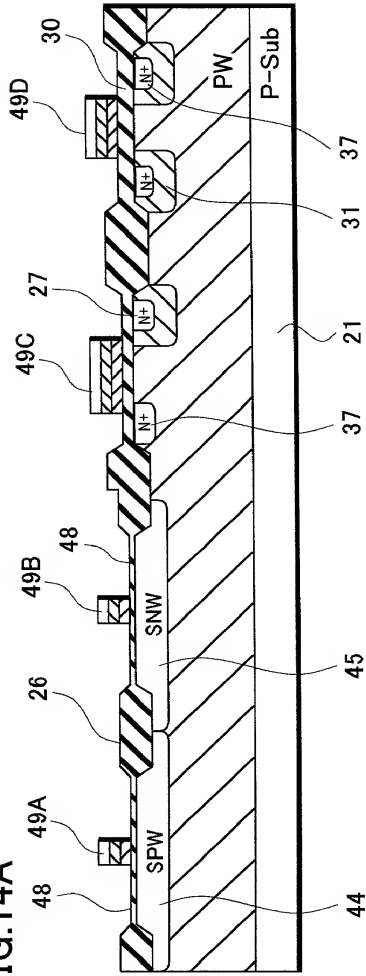


FIG. 14B

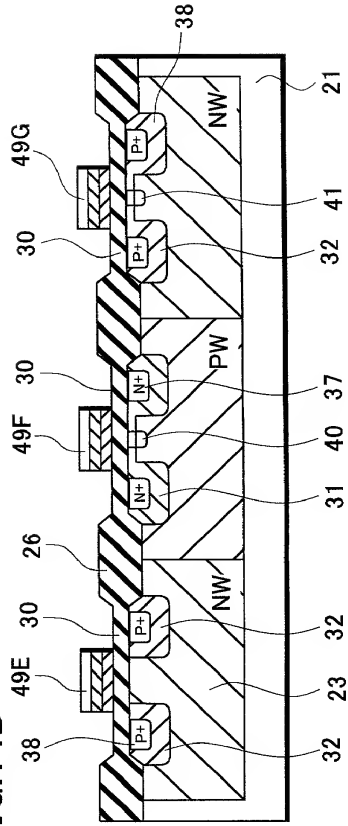


FIG. 15A

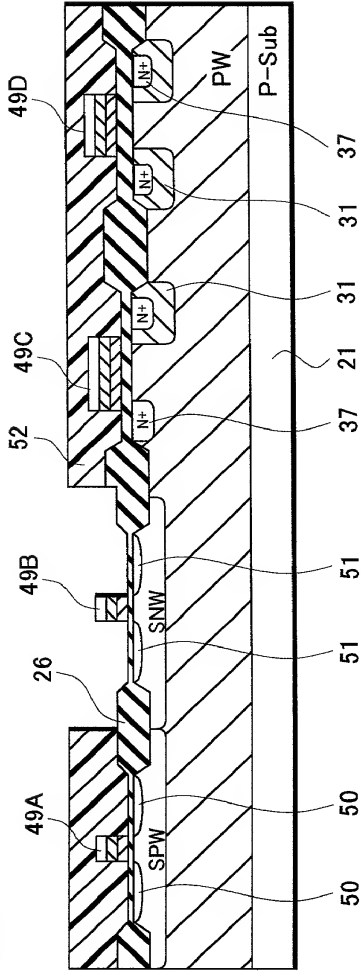


FIG. 15B

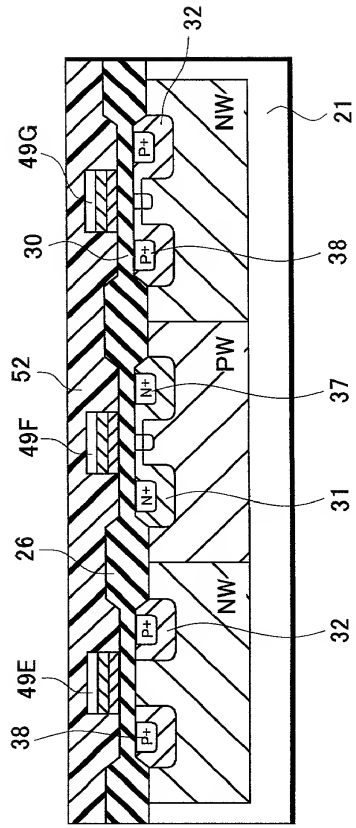


FIG. 16A

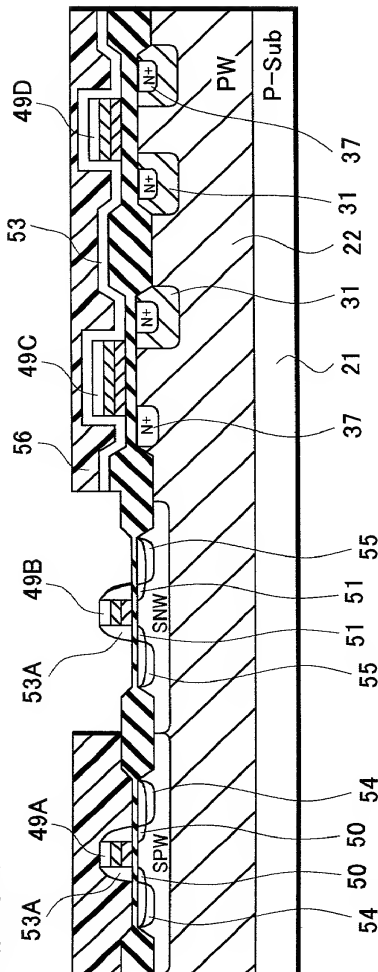


FIG. 16B

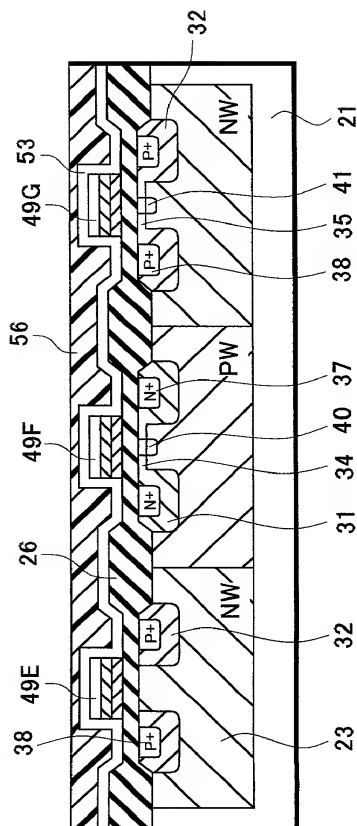




FIG.17A

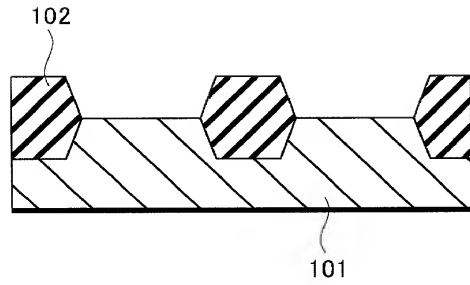


FIG.17B

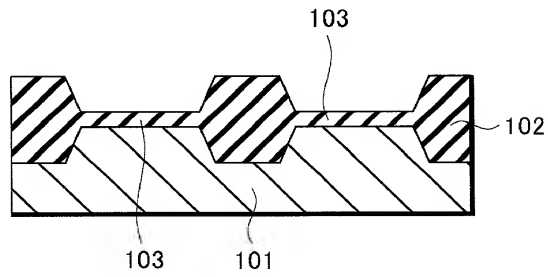


FIG.17C

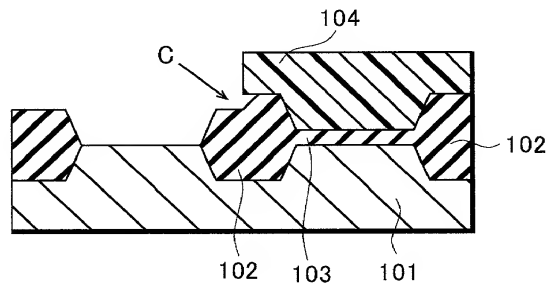


FIG.18A

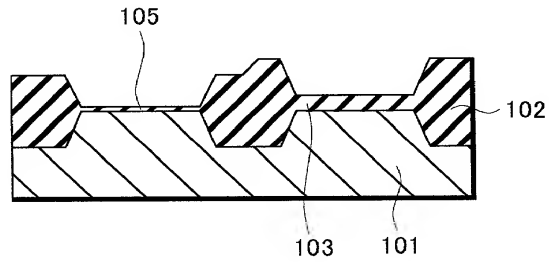


FIG.18B

